Fig-1

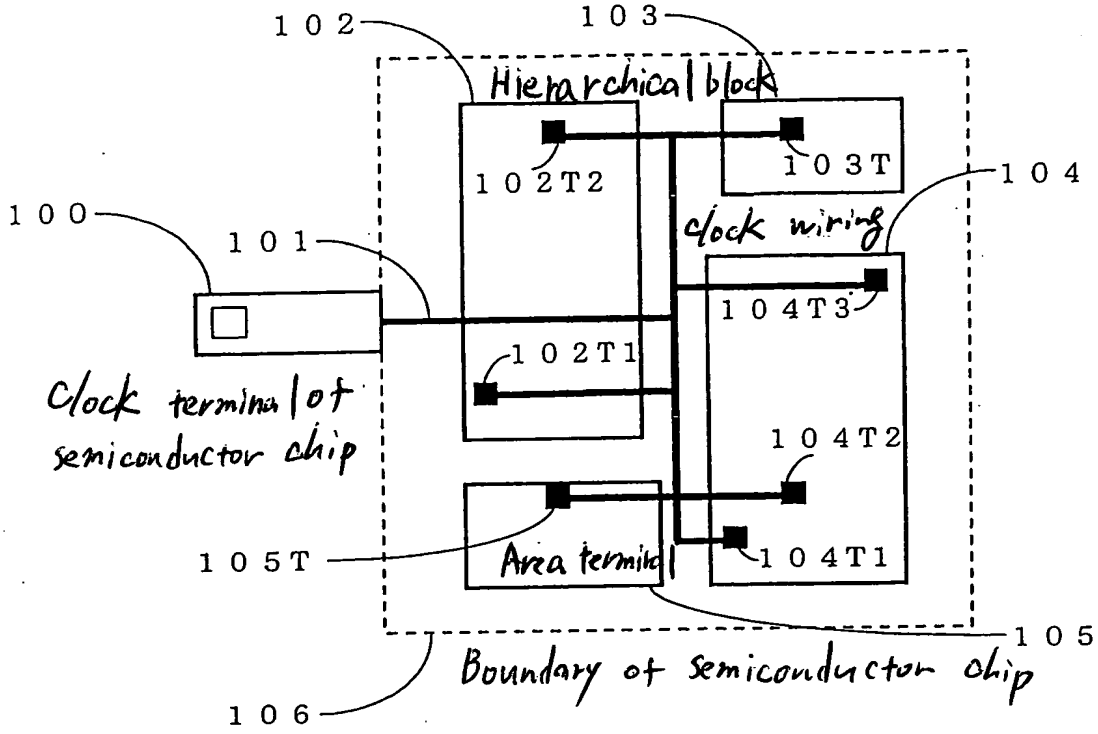

102
103
Hierarchical block
102T2
103T
104
100
101
clock wiring
104T3
102T1
Clock terminal of semiconductor chip
104T2
105T
Area terminal
104T1
105
106
Boundary of semiconductor chip

Fig. 2

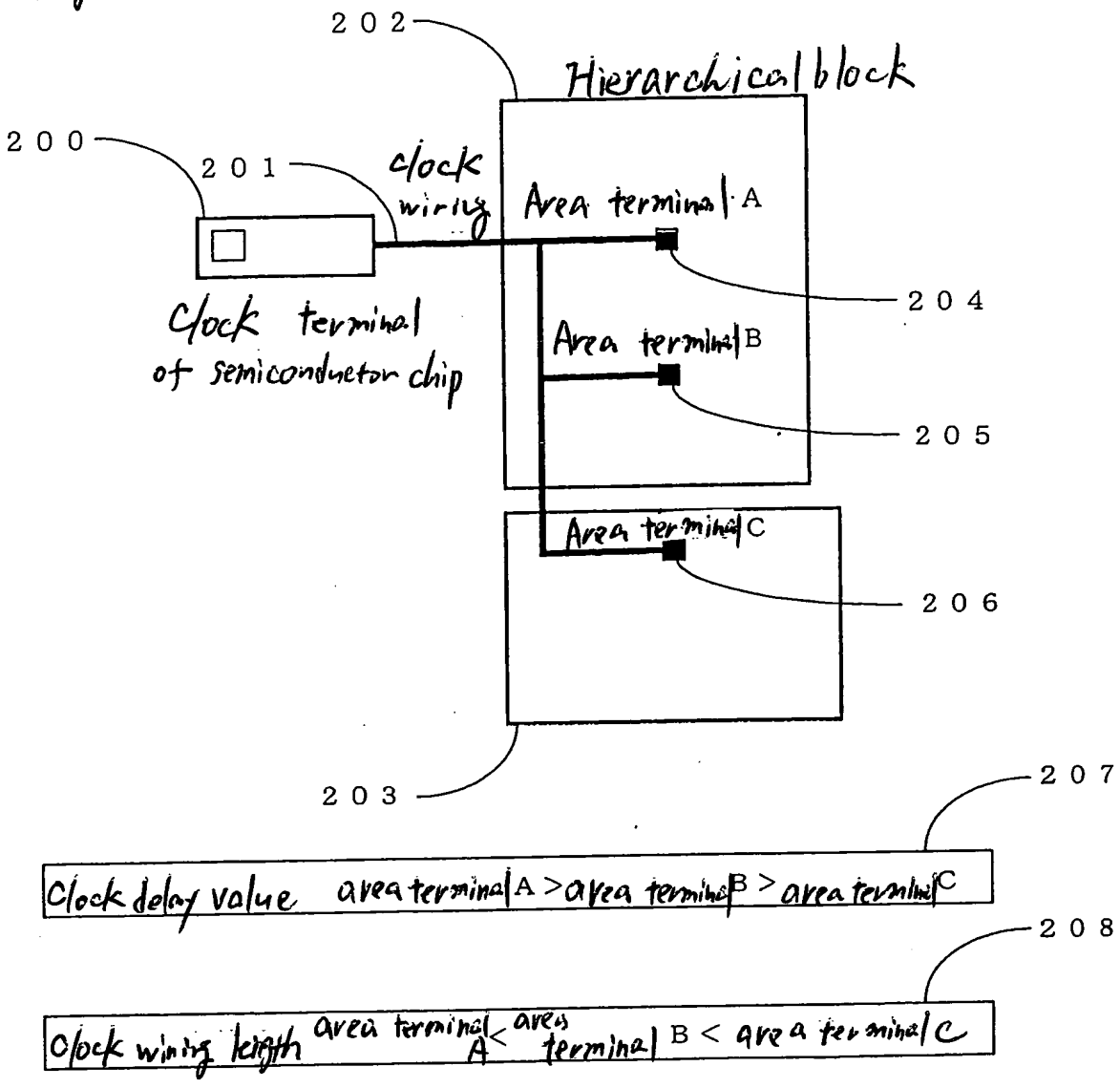

202
Hierarchical block
200
201
clock wiring
Area terminal A
204
Clock terminal of semiconductor chip
Area terminal B
205
Area terminal C
206
203
207
Clock delay value area terminal A > area terminal B > area terminal C
208
Clock wiring length area terminal A < area terminal B < area terminal C

Fig.3

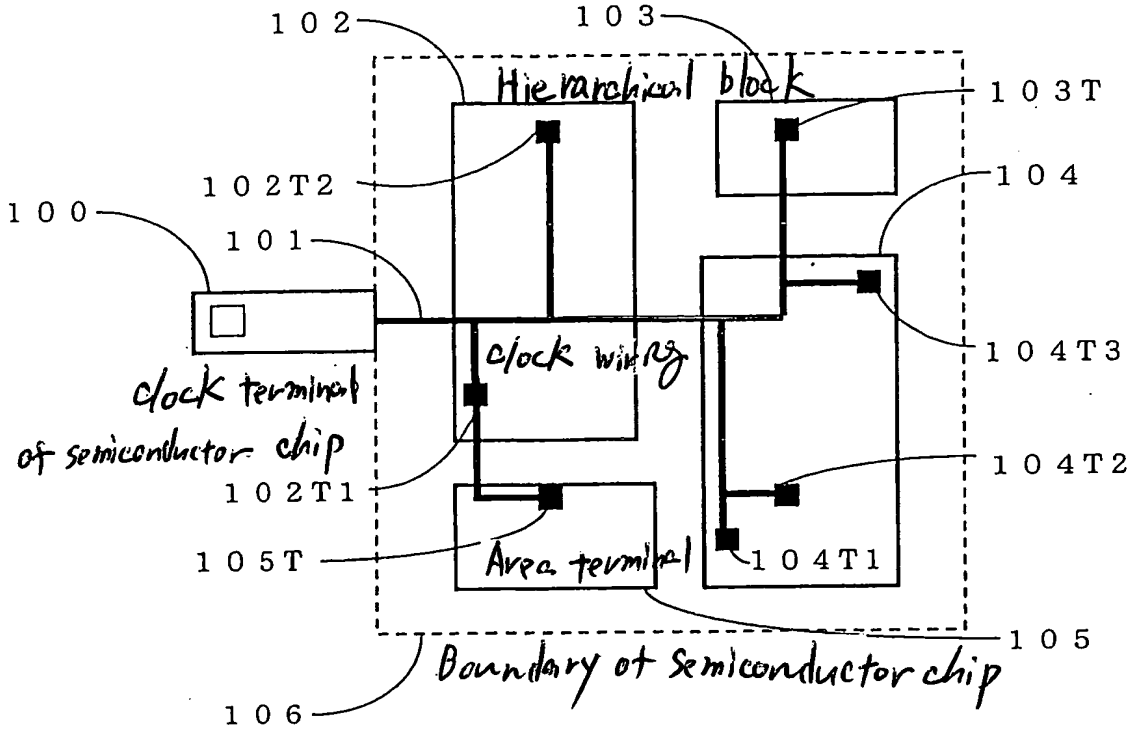

102
103
Hierarchical block
103T
102T2
104
100
101
104T3
clock wiring
clock terminal
of semiconductor chip
102T1
104T2
105T
Area terminal
104T1
105
Boundary of semiconductor chip
106

Fig.4

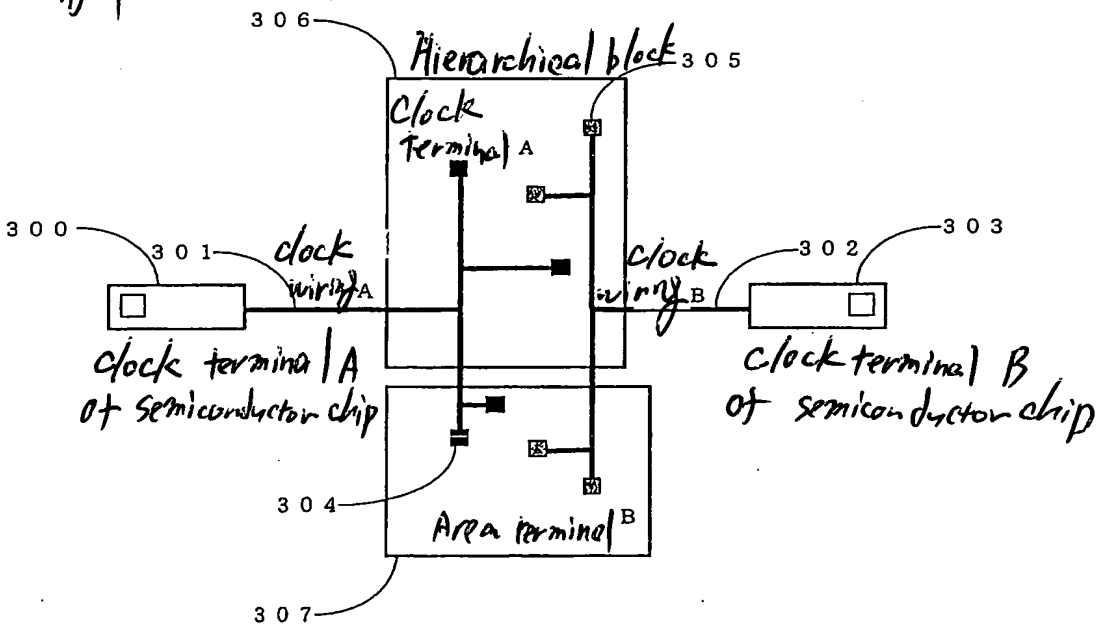

306
Hierarchical block
305
Clock
Terminal A
300
301
clock
wiring A
clock
wiring B
302
303
clock terminal A
of semiconductor chip
clock terminal B
of semiconductor chip
304
Area terminal B
307

Fig.5

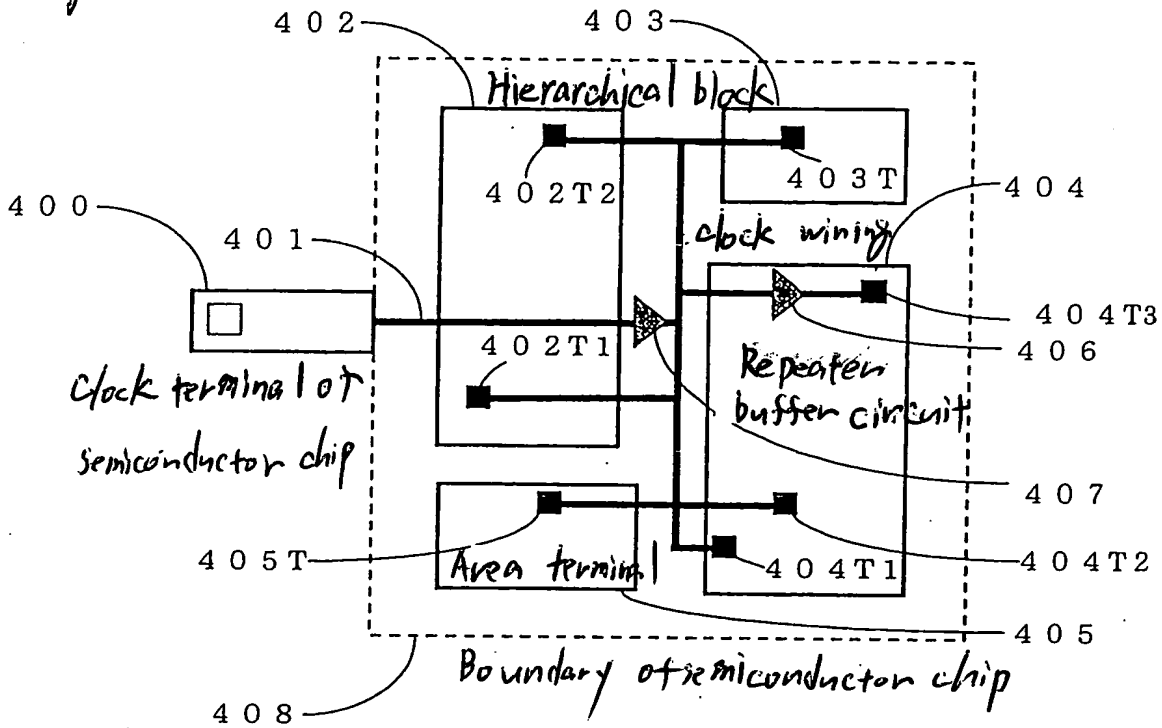

402
403
Hierarchical block
402T2
403T
400
401
404
clock wiring
404T3
406
402T1
Repeater buffer circuit
clock terminal of semiconductor chip
407
405T
Area terminal
404T1
404T2
405
Boundary of semiconductor chip
408

Fig.6

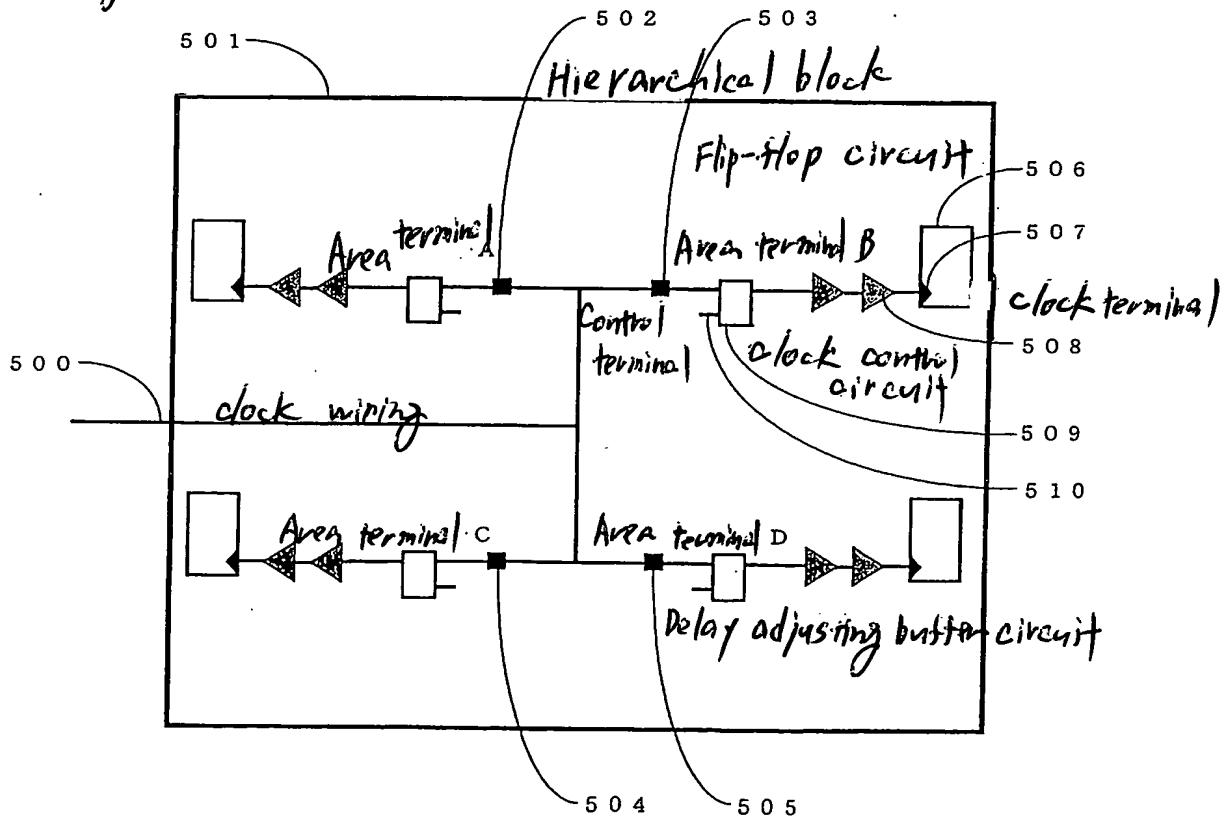

501
502
503
Hierarchical block
Flip-flop circuit
506
Area terminal A
Area terminal B
507
clock terminal
control terminal
508
500
clock wiring
clock control circuit
509
510
Area terminal C
Area terminal D
Delay adjusting buffer circuit
504
505

Fig. 17

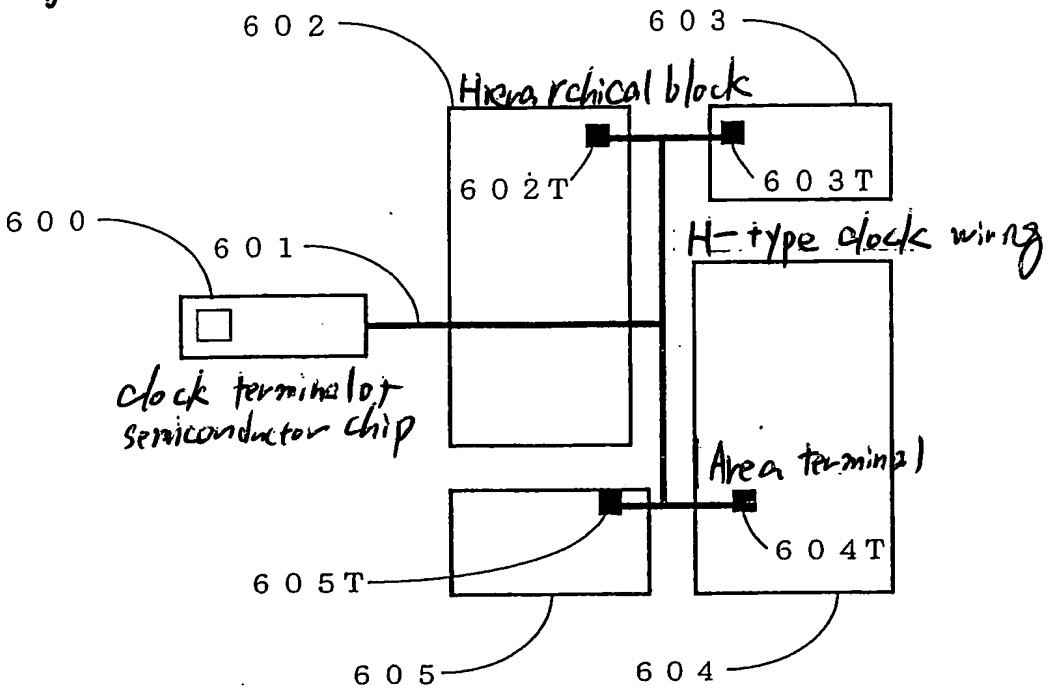
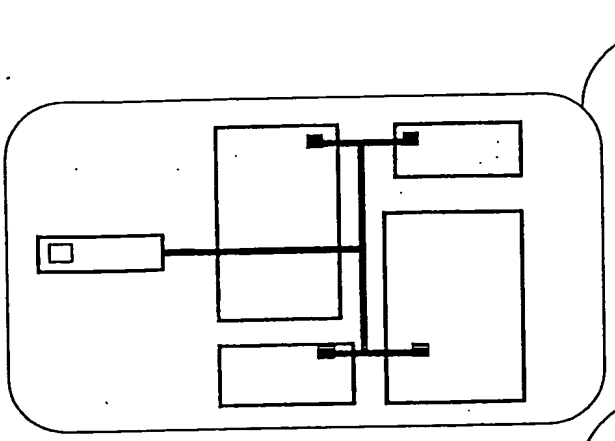
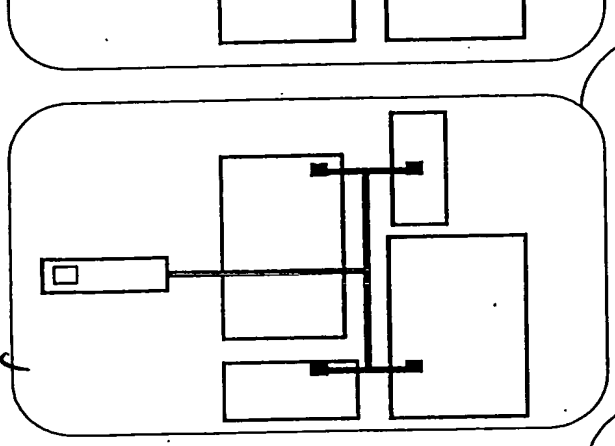

602
603
Hierarchical block
602T
603T
600
601
H-type clock wiring
clock terminal of semiconductor chip
Area terminal
604T
605T
605
604

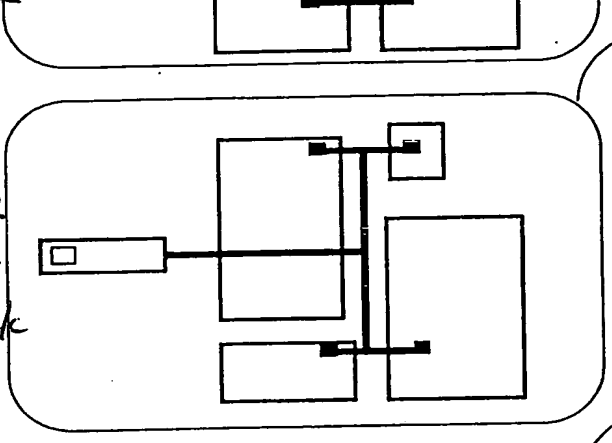
Fig. 8



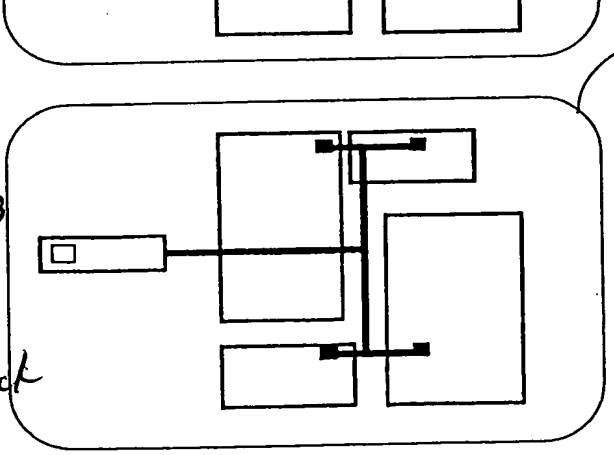
Floor plan original form



Floor plan correction 1
Rotation of hierarchical block



Floor plan correction 2
change in size of hierarchical block



Floor plan correction 3
change in arrangement position of hierarchical block

Fig.9

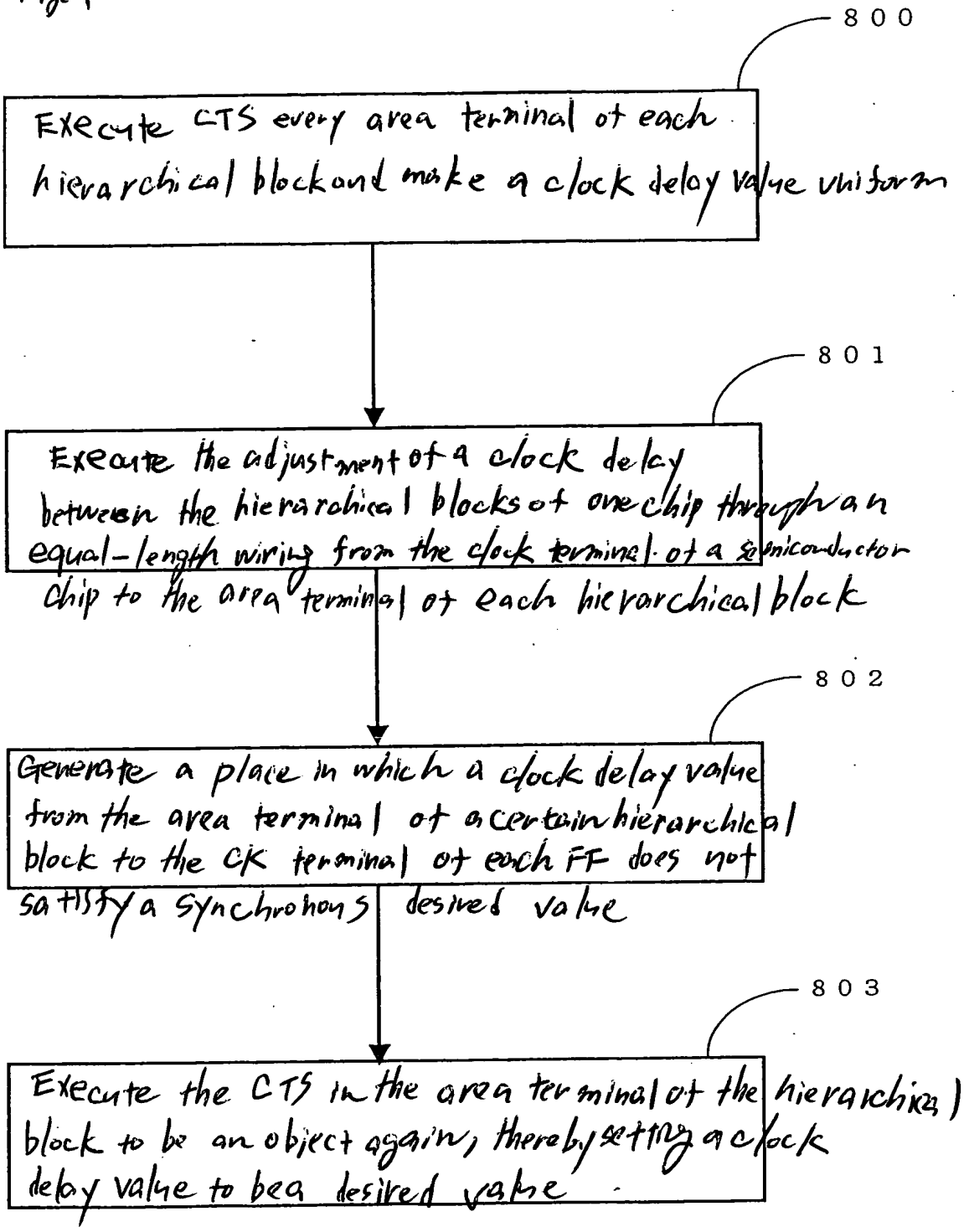
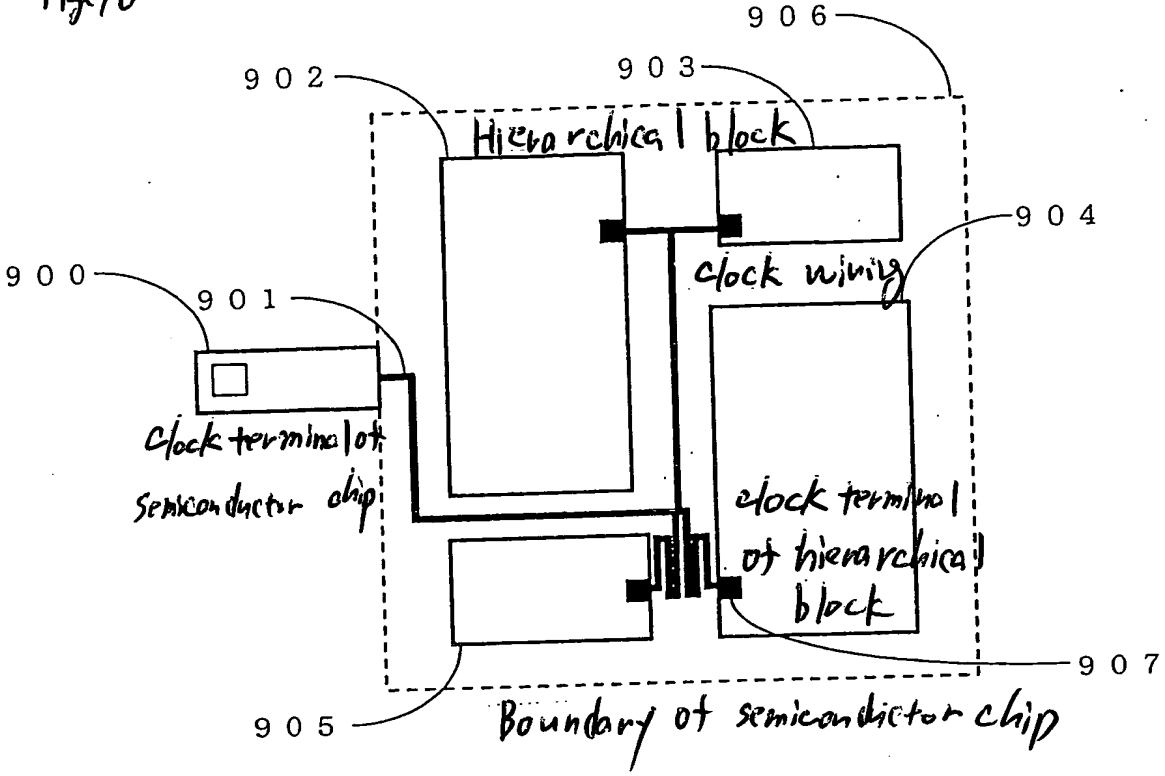

800
Execute CTS every area terminal of each hierarchical block and make a clock delay value uniform
801
Execute the adjustment of a clock delay between in the hierarchical blocks of one chip through an equal-length wiring from the clock terminal of a semiconductor chip to the area terminal of each hierarchical block
802
Generate a place in which a clock delay value from the area terminal of a certain hierarchical block to the CK terminal of each FF does not satisfy a synchronous desired value
803
Execute the CTS in the area terminal of the hierarchical block to be an object again, thereby setting a clock delay value to be a desired value

Fig 10


906
902
903
Hierarchical block
904
clock wiring
900
901
clock terminal of semiconductor chip
clock terminal of hierarchical block
907
905
Boundary of semiconductor chip